

What is claimed is:

1. A display device having thin film transistors on a substrate thereof, wherein

the display device includes gate patterns in each of which
5 a gate line and a gate electrode of the thin film transistor are integrally formed,

the gate pattern is constituted by at least three-layered films consisting of a lowermost layer, an intermediate layer formed of at least one layer and an uppermost layer at least
10 at either a portion of the thin film transistor or a portion of the gate pattern which crosses a drain line,

the intermediate layer is formed of a material selected from the group consisting of pure Al, an Al alloy, pure Ag, an Ag alloy, pure Cu and a Cu alloy, and the uppermost layer and
15 the lowermost layer are formed of a metal having a melting point higher than a melting point of the material of the intermediate layer, and

end portions of the intermediate layer are retracted from end portions of the uppermost layer and end portions of the
20 lowermost layer.

2. A display device according to claim 1, wherein the uppermost layer and the lowermost layer are formed of pure Mo or an Mo alloy.

3. A display device according to claim 1, wherein the
25 uppermost layer and the lowermost layer are formed of an Mo-W

alloy.

4. A display device according to claim 1, wherein end portions of the uppermost layer are retracted from end portions of the lowermost layer.

5 5. A display device according to claim 1, wherein the thin film transistor includes a semiconductor layer and the gate electrode is arranged above the semiconductor layer.

6. A display device according to claim 1, wherein the thin film transistor includes a polycrystalline semiconductor layer.

10 7. A display device having thin film transistors on a substrate thereof, wherein

the display device includes gate patterns in each of which a gate line and a gate electrode of the thin film transistor are integrally formed, and an insulation film which covers the
15 gate patterns,

the gate pattern is constituted by at least three-layered films consisting of a lowermost layer, an intermediate layer formed of at least one layer and an uppermost layer at least at either one of a portion of the thin film transistor or a portion
20 of the gate pattern which crosses a drain line,

the intermediate layer is formed of a material selected from the group consisting of pure Al, an Al alloy, pure Ag, an Ag alloy, pure Cu and a Cu alloy, and the uppermost layer and the lowermost layer are formed of a metal having a melting point
25 higher than a melting point of the material of the intermediate

layer, and

end portions of the uppermost layer of the gate electrode are retracted from end portions of the lowermost layer and, at the same time, end portions of the intermediate layer of the gate electrode are retracted from end portions of the uppermost layer and end portions of the lowermost layer.

8. A display device according to claim 7, wherein the thin film transistor includes a semiconductor layer and the gate electrode is arranged above the semiconductor layer.

10 9. A display device according to claim 8, wherein the uppermost layer and the lowermost layer are formed of pure Mo or an Mo alloy.

10. A display device according to claim 8, wherein the uppermost layer and the lowermost layer are formed of an Mo-W alloy.

11. A display device according to claim 8, wherein the uppermost layer and the lowermost layer are formed of an Mo alloy, and an etching rate of the Mo alloy of the uppermost layer is faster than an etching rate of Mo alloy of the lowermost layer.

20 12. A display device according to claim 11, wherein the lowermost layer is formed of an Mo-Cr alloy and the uppermost layer is formed of an Mo-W alloy.

13. A display device according to claim 7, wherein the semiconductor layer includes an LDD region, and the lowermost layer of the gate electrode has at least a portion thereof

overlapped with the LDD region.

14. A display device according to claim 7, wherein the thin film transistor includes a polycrystalline semiconductor layer.

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